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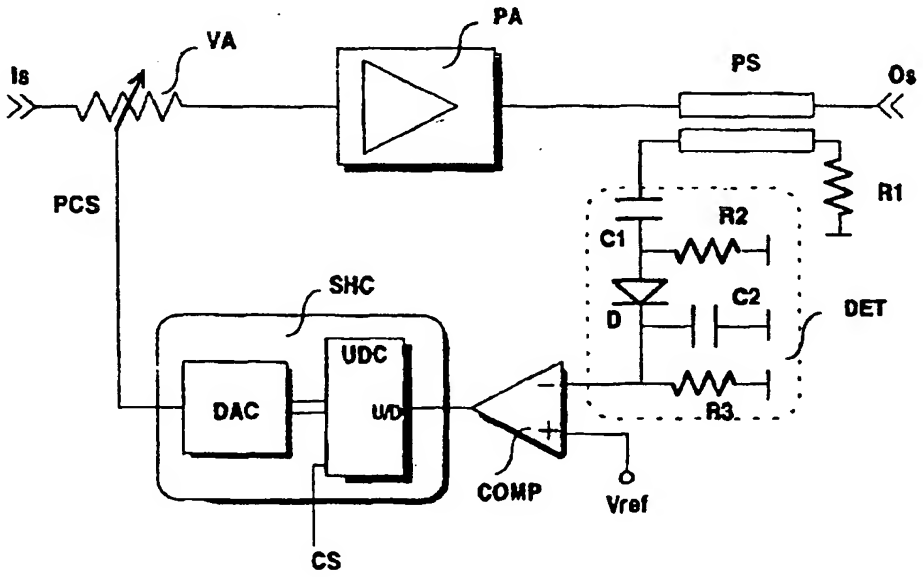

(57) Abstract

Output power control in burst transmitters that comprise a power amplifier stage the gain of which varies according to a power control signal (PCS), an output signal sensing circuit (PS), a detector (DET) that generates a DC voltage signal proportional to the level of the sensed signal and a comparator (COMP) to generate the power control signal (PCS) in proportion to the difference between the DC voltage coming from the detector (DET) and a reference voltage (Vref). The power control signal (PCS) is sampled in a sample-and-hold circuit (SHC) using the active edges of a clock signal (CS), these occurring only at the moments when there are signal bursts to be transmitted and at a time subsequent to the start of each burst greater than the duration of the transient of the DC analogue voltage signal at the output of the detector.

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OUTPUT POWER CONTROL IN BURST TRANSMITTERS

OBJECT OF THE INVENTION

This invention concerns power transmitters for radiofrequency signals in which the signal to be transmitted consists of bursts, consequently there are many periods when this signal is zero.

The power control presented here permits the mean power of the output signal to be kept constant and controlled during the bursts, irrespective of the relationship between the periods of burst transmission and the periods between bursts when the signal is zero.

BACKGROUND OF THE INVENTION

The need to maintain the output signal power steady from power amplifiers in radiofrequency transmitters, means these transmitters must incorporate some control mechanism which ensures this requirement irrespective of such major factors such as input signal power, power amplifiers gain, variations in this gain with temperature, ageing, etc.

This control is normally achieved by means of a power feedback loop. This loop is based on detecting the output power of the final power amplifier, obtaining a signal proportional to this output power for comparison with a stable reference in a differential amplifier, the output of which generates a power control signal which is used to modify the gain in one of the amplifier stages.

In this way a potential increase in output power is converted into a decrease in the amplifier gain, offsetting the increase mentioned and thereby maintaining the output power constant.

An example of the foregoing can be seen in the European patent application EP 0462773.

The output power detector is usually a directional coupler with a load resistor and a rectifier. Afterwards there is a lowpass filter with a fairly narrow bandwidth such that the value obtained at its output does not fluctuate and therefore does not introduce amplitude modulation in the output signal.

Moreover, in burst transmitters, the preceding principle is not applicable as such because the reading would be in error through calculating the mean value of output power taking into consideration the zero signal periods and would be further impaired when the system permits,

according to the level of occupancy of the channels, the omission of bursts in the frame formed by the burst assembly.

The patent application mentioned above proposes a solution to this problem by applying to one of the differential amplifier inputs, instead of a fixed reference voltage, a pulse signal which takes a determined steady value during the periods of transmission of each burst and a zero or very low value for the rest.

Nevertheless this alternative does not overcome the problem arising particularly when the gain of the differential amplifier is very large, since any voltage offset in the amplifier or detector, no matter how small, would saturate the differential amplifier, causing the power amplifier to adopt one of its extreme positions (maximum gain or minimum gain) in the absence of an input signal. This would result in a transient in the output signal power at the start of each burst until the loop could force the power amplifier to its equilibrium working point. How long this transient is, would depend on the bandwidth of the lowpass filter of the output power detector, among other things.

During this transient period, the output signal would therefore suffer amplitude modulation, which has a very harmful effect on the communications established.

CHARACTERISATION OF THE INVENTION

This invention is intended for overcoming the drawbacks mentioned above in burst transmitters, the latter comprising a power amplifier stage whose gain is varied in accordance with a power control signal, means for sensing the output signal, a detector that produces a DC voltage signal proportional to the level of the sensed signal and a differential amplifier to generate the power control signal in proportion to the difference between the DC voltage from the detector and a reference voltage.

The power control signal mentioned is sampled in a sample-and-hold circuit using the active edges of a clock signal, these occurring only at the instants when there are burst signals to be transmitted and at a time subsequent to the start of each burst greater than the duration of the transient of the DC analogue voltage signal at the output of the detector.

BRIEF FOOTNOTES TO THE FIGURES

A fuller explanation of the invention can be found in the following

description of a preferred implementation based on the figures attached, in which:

- figure 1 shows a block diagram of an output power control circuit in accordance with the state of the art,
- figure 2 is the output power control circuit according to the invention,
- figure 3 shows a circuit like the previous one but in which the attenuator employed is of the digital type, and
- figure 4 shows time domain diagrams of various signals at points in the power control feedback loop.

DESCRIPTION OF ONE WAY OF IMPLEMENTING THE INVENTION

Below is given a description of an implementation of the power control circuit that makes use of the principle according to the invention object of this patent.

The output power control is based on a known technique that is represented by the block diagram as shown in figure 1.

Thus, there is a power amplification stage PAS, of variable gain, which receives an input signal Is and which boosts the power of the output signal Os by a determined factor termed the power gain.

A small sample of this output signal Os is taken by means of an output signal sensing circuit PS, which is applied to a power detector DET which, in turn, produces a baseband signal proportional to the mean power of the output signal Os, whereby this baseband signal can be subsequently used to perform control of the power in the output signal Os by means of a feedback process.

The output signal from the detector DET is applied to one of the inputs of a comparator COMP which receives, through its other input, a reference voltage Vref, the output signal from this comparator COMP being proportional to the difference between the two input signals, that coming from the detector DET and the reference voltage Vref.

This output signal from the comparator COMP is a power control signal PCS that is applied to the power amplifier stage PAS to vary its gain such that, by means of the feedback loop so formed, an increase in the mean power of the output signal Os results in a decrease in the gain of the preceding power amplifier stage PAS and, through this, a decrease in the

power of the output signal that offsets the initial increment.

As a consequence of this, a balanced control of the output signal Os of the power amplifier is achieved against possible variations in or tolerances of the components and signals existing in the assembly.

When the signal that is applied to the power amplifier stage PAS is not steady but, as is shown in figure 4.a, formed by bursts, its mean power has to be calculated by means of lowpass filtering with a very narrow bandwidth and a very large time constant since, otherwise, amplitude modulation would be introduced in the output signal, which is extremely harmful. Figure 4.b shows the waveform of the power signal detected in a situation where the time constant of the lowpass filter of the detector is not very large.

When the lowpass filtering is done with a very large time constant, the output signal from the detector is practically a continuous signal, thereby avoiding the amplitude modulation of the output signal from the amplifier; nevertheless, this mean value of the detected output power is not correct since it does not depend only on the mean power of the bursts, but also on the actual presence of these bursts. Thus, the output of each burst is not constant but depends on the occupancy level, or number of bursts present, in the transmitted frames.

Figure 2 shows the solution proposed by this invention in order to make the power control independent of the level of occupancy of the frames. In this power control, the power amplifier stage is formed by a non-linear power amplifier PA of fixed gain, preceded by a variable attenuator VA such that the overall gain of the assembly is also variable.

The variable attenuator VA offers an attenuation that depends on the value of the power control signal PCS, it being approximately proportional to this value. This attenuator consists of a PIN type diode connected between the signal line and ground, such that it presents a resistance to ground that depends on its bias voltage. The greater the forward bias voltage, the less the resistance presented to ground is and, consequently, the greater the attenuation presented to the signal being transmitted along the line is.

The power sensing circuit PS is formed by a two-line microstrip directional coupler. The coupling loss of this device is, for the present case, 30 dB and it is loaded with a resistance R1 of 50 Ω.

To the other extremity is connected the detector DET; at its input this has a highpass filter C1, R2 with a cutoff frequency below the working frequency of the amplifier. Afterwards there is a detecting diode D and a lowpass filter C2, R3, the time constant of which is about ten times less than the duration of the bursts.

The output signal from this detector DET is applied to the inverting input of the comparator COMP, the non-inverting input being connected to the reference voltage Vref. The output signal from this comparator COMP takes a value of 5 V, or logical 1, when the output signal of the detector is less than the reference voltage, it being 0 V, or logical 0, otherwise.

The output signal of the aforementioned comparator COMP is applied to a sample-and-hold circuit SHC which, in this case, is formed by a digital up/down counter UDC and a digital-to-analogue converter DAC.

The digital up/down counter UDC receives, as a clock signal, a control signal CS consisting of pulses, the presence of which corresponds to the appearance of transmitted bursts and the width of which is equal to one half of burst duration. Thus, the falling edge of these pulses which is considered to be the clock active edge, coincides with the centre of each burst.

This digital up/down counter UDC also receives the output signal from the comparator COMP at its up/down count input. In this way the count value stored in it is increased by one unit when an active clock pulse edge appears, that is, in the centre of each burst, and, in addition, the output voltage of the detector DET is greater than the reference voltage Vref; otherwise there is a decrease.

The outputs of this up/down counter UDC are applied to the digital-to-analogue converter DAC where an output voltage is produced that is proportional to the value stored in the up/down counter UDC mentioned and which is termed the power control signal PCS, as already stated.

This power control signal PCS is applied to the control input of the variable attenuator VA, which offers an attenuation in the incoming signal path which becomes greater as the power control signal increases.

When use is made of a digitally controlled variable attenuator, then there is no need for a digital-to-analogue converter, as is shown in figure 3, and the digital output of the up/down counter UDC is applied directly to the

attenuator VA mentioned.

In this way, the power control loop permits true control of the mean transmitted power calculated in each burst, irrespective of the appearance or not of a given burst without this affecting the mean value mentioned. This also permits the filter employed for calculating the mean value of the transmitted power to have a much faster response, as can be seen in figure 4.c, and the control to be active for a very short time.

When the loop is balanced, the output of the comparator COMP takes the values of logical 1 and 0 alternatively, which makes the power control signal PCS oscillate between two values, as can be seen from figure 4.d, the proximity of these two values becoming greater as the number of bits employed by the digital up/down counter UDC and by the digital-to-analogue converter DAC becomes greater.

This last situation can be avoided by making the digital-to-analogue converter DAC not use the two bits of least weight from the counter.

A very large number of bits in the digital-to-analogue converter DAC permits the power of the output signal to be kept within a very narrow range, though it implies that the initial system response is very slow; this can be improved if the initial value of the counter is pre-established in accordance with calculations made which depend on the rest of the parameters of the loop.

CLAIMS

1.- **OUTPUT POWER CONTROL CIRCUIT FOR BURST TRANSMITTERS** that comprise a power amplifier stage (PAS) the gain of which varies according to a power control signal (PCS), an output signal sensing circuit (PS), a detector (DET) that generates a DC voltage signal proportional to the level of the sensed signal and a comparator (COMP) to generate the power control signal (PCS) in proportion to the difference between the DC voltage coming from the detector (DET) and a reference voltage (Vref) **characterised** in that it also comprises a sample-and-hold circuit (SHC) which receives a clock signal (CS) and which samples the power control signal (PCS) only at the moments when there are signal bursts to be transmitted.

2.- **OUTPUT POWER CONTROL CIRCUIT** according to claim 1, **characterised** in that the sampling of the power control signal is realized at a time subsequent to the start of each burst greater than the duration of the transient of the DC analogue voltage signal at the output of the detector (DET).

3.- **OUTPUT POWER CONTROL CIRCUIT** according to claim 1, **characterised** in that the sample-and-hold circuit (SHC) comprises:

- a digital up/down counter (UDC) which receives the clock signal (CS) and to which is applied as the up/down count control signal (U/D) the output signal from the comparator (COMP), and

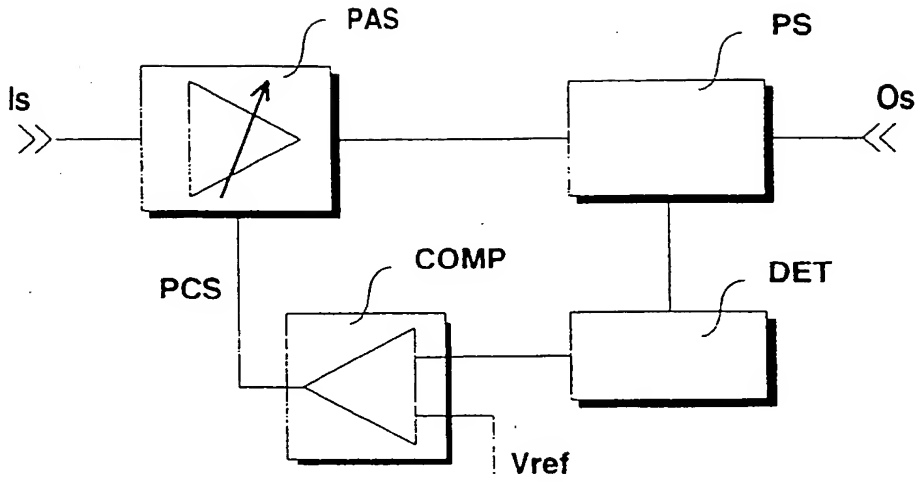
- a digital-to-analogue converter (DAC) which receives the output of the digital counter (UDC) and whose analogue output signal is applied to the variable power amplifier stage as the power control signal (PCS).

4.- **OUTPUT POWER CONTROL CIRCUIT** according to claim 3 **characterised** in that the power amplifier stage (PAS) comprises a power amplifier (PA) preceded by a variable attenuator (VA), the attenuation of which varies in accordance with the power control signal (PCS).

5.- **OUTPUT POWER CONTROL CIRCUIT** according to claim 4 **characterised** in that the variable attenuator (VA) is digitally controlled and directly receives the output signal from the digital up/down counter (UDC), there being no need to use a digital-to-analogue converter.

6.- **OUTPUT POWER CONTROL METHOD FOR BURST TRANSMITTERS** **characterised** in that it comprises the stages of:

- extraction of a small part of the transmitter output signal,
- detection of the mean power of this extracted signal,
- comparison of the detected mean power with a reference signal,
- sampling and holding, with a clock signal, of the value of the comparison previously performed, and
- variation in the gain of the amplifier stage of the main signal in accordance with the value of the signal coming from the preceding sample-and-hold process.


PAS
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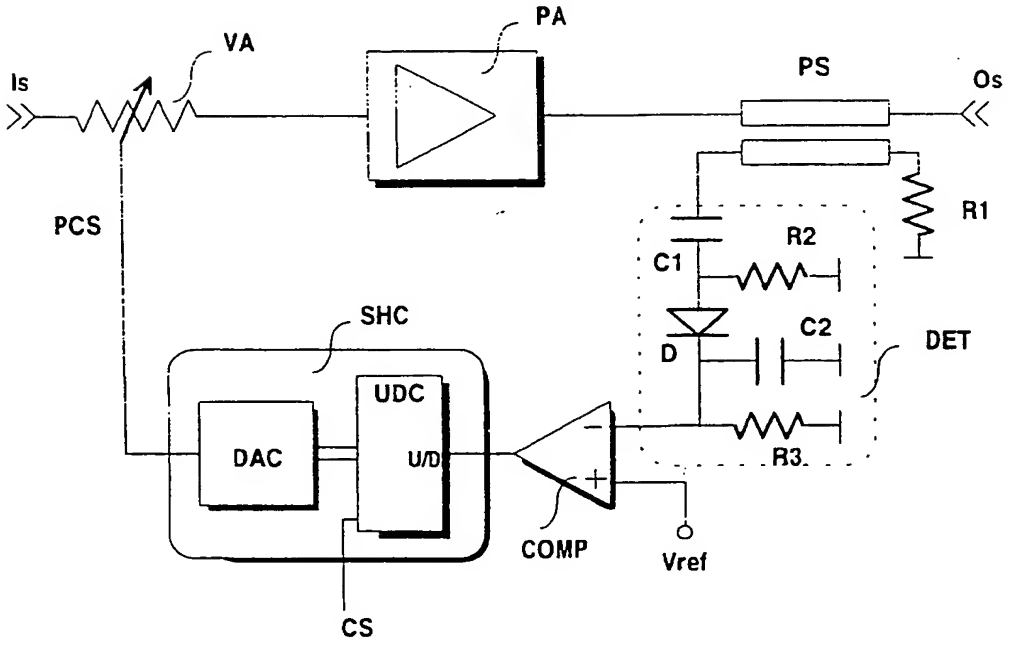
Is
Os
COMP
PCS
DET
Vref

Fig. 1


PA
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COMP
Vref
CS

Fig. 2

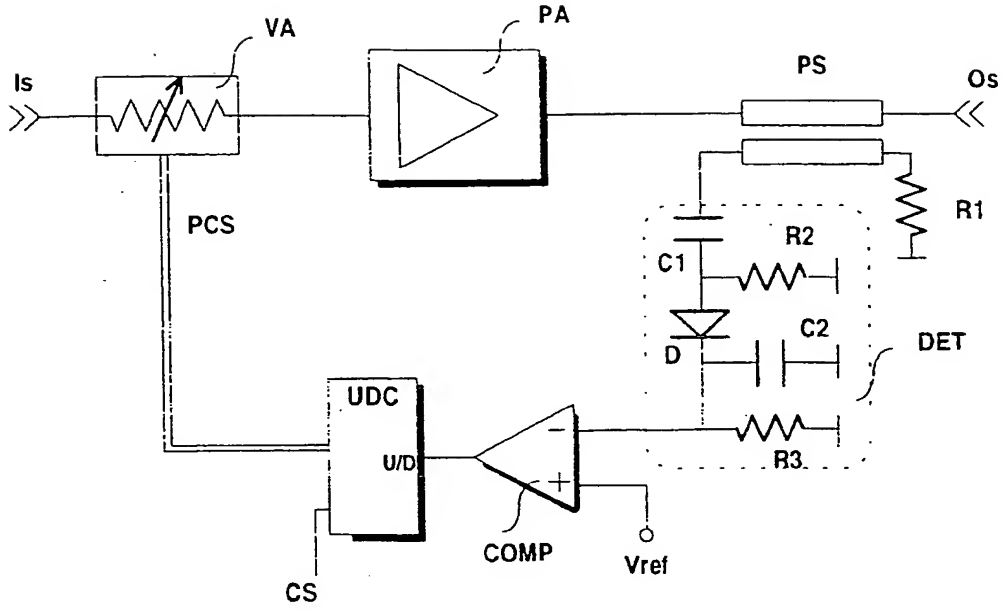

Fig. 3

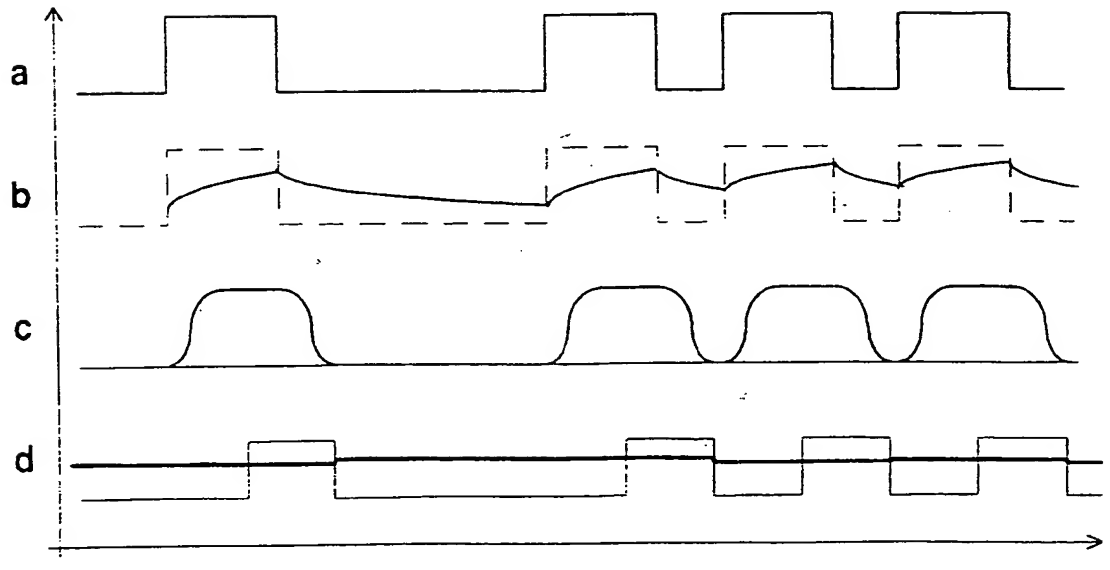

Fig. 4

INTERNATIONAL SEARCH REPORT

Inte onal Application No
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A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H03G3/30

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

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IPC 6 H03G

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 010, no. 384 (E-466), 23 December 1986 & JP 61 173507 A (NEC CORP), 5 August 1986, see abstract ---	1-4,6
P,X	EP 0 688 108 A (MITSUBISHI ELECTRIC CORP) 20 December 1995 see abstract ---	1-4,6
X	EP 0 535 669 A (MATSUSHITA ELECTRIC IND CO LTD) 7 April 1993 see abstract ---	1

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[X] Further documents are listed in the continuation of box C.

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A	US 3 969 683 A (FABRICIUS WAYNE NIXON) 13 July 1976 see abstract; figures 1,1A	5
A	EP 0 632 585 A (ALCATEL TELSPACE) 4 January 1995	1-6
A	EP 0 509 733 A (MITSUBISHI ELECTRIC CORP) 21 October 1992	1-6

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Information on patent family members

Int ional Application No
PCT/EP 96/03313

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
EP-A-0688108	20-12-95	JP-A-	8008768	12-01-96
		US-A-	5566363	15-10-96
EP-A-0535669	07-04-93	JP-A-	5095295	16-04-93
		DE-D-	69209206	25-04-96
		DE-T-	69209206	02-10-96
		US-A-	5369789	29-11-94
US-A-3969683	13-07-76	CA-A-	1080815	01-07-80
		DE-A-	2617114	11-11-76
		DE-C-	2660662	23-09-82
		FR-A-	2308972	19-11-76
		GB-A-	1530183	25-10-78
		JP-A-	51128248	09-11-76
EP-A-0632585	04-01-95	FR-A-	2708399	03-02-95
		CA-A-	2126919	31-12-94
		JP-A-	7079125	20-03-95
		US-A-	5430410	04-07-95
EP-A-0509733	21-10-92	JP-A-	4316205	06-11-92
		US-A-	5208550	04-05-93